REMARKS

Status of Claims

Claims 1 and 3 – 16 remain pending in the present application. Claim 2 was previously canceled, and Claims 17 – 30 are canceled in the above amendment, as non-elected in consideration of a restriction previously issued by the Examiner. Claims 1 and 3 have been amended to more clearly defined over the prior art cited.

Claims Rejected under 35 U.S.C. § 103

The Examiner has again rejected Claims 1, and 10-16 as being unpatentable over Van Hook et al. (U.S. Patent No. 6,342,892 – hereinafter "Van Hook") in view of Ezer et al. (U.S. Patent No. 6,274,239 – hereinafter "Ezer"). The Examiner states that Van Hook teaches all that is recited in Claims 1 and 16 "except that the vector unit obtains from the texture cache a vector of at least one partition of the multimedia." The Examiner relies on Ezer for teaching an integrated media coprocessor chip that partitions 3-D graphics, video, and audio tasks through time division multiplexing and which includes texture memory buffers 425 in a display processor 203 to source image data used for texturing and which are shared between texture mapping and MPEG video processing. For the reasons noted below, applicants respectfully disagree that the art cited reads on their claims, particularly, in view of the amendments made above, which more clearly distinguish over the cited art.

In the interest of reducing the complexity of the issues for the Examiner to consider in this response, the following discussion focuses on independent Claim 1 and dependent Claim 3. The patentability of each remaining dependent claim is not necessarily separately addressed in detail. However, applicants' decision not to discuss the differences between the cited art and each dependent claim should not be considered as an admission that applicants concur with the Examiner's conclusion that these dependent claims are not patentable over the disclosure in the cited references. Similarly, applicants' decision not to discuss differences between the prior art and every claim element, or every comment made by the Examiner, should not be considered as an admission that applicants concur with the Examiner's interpretation and assertions regarding those claims. Indeed, applicants believe that all of the dependent claims patentably distinguish over the references cited. Moreover, a specific traverse of the rejection of each dependent claim is not

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required, since dependent claims are patentable for at least the same reasons as the independent claims from which the dependent claims ultimately depend.

Significant Differences between Cited Art and Applicants' Claims

As amended, Claim 1 is now directed to "a programmable graphics pipeline for processing and rendering variable length multimedia data, wherein different types of multimedia data are divided into partitions of differing lengths." In contrast, Van Hook teaches a coprocessor 200, which is coupled to a main processor 100, and which includes both a signal processor 400 and a separate display processor 500. As indicated by Van Hook at column 7, lines 21-27:

> The signal processor 400 and display processor 500 work independently, but the signal processor can supervise the display processor by sending graphics commands to it. Both signal processor 400 and display processor 500 can be controlled directly by main processor 100.

Furthermore, Van Hook does not teach or suggest that signal processor 400 is actually used in a graphics pipeline for rendering multimedia data. Instead, the reference teaches that the signal processor is principally employed for specific signal processing functions, and these functions are listed at column 20, line 60 through column 21, line 6. It will be noted that these listed functions do NOT include ***rendering*** variable length multimedia data. Although display processor 500 is employed for rendering images, in rejecting Claim 1, the Examiner has cited signal processor 400 in combination with the media coprocessor disclosed by Ezer. Clearly, for the reasons noted below, Van Hook's signal processor 400, even when modified to include elements of the digital signal processor or display processor disclosed by Ezer, does not result in a programmable graphics pipeline as recited by applicants' claims.

The Examiner has also indicated that Van Hook teaches "a texture memory 502 as shown in Fig. 6." However, display processor 500 (which includes texture memory 502) is not part of signal processor 400 and does not include and is not coupled to the other elements referenced by the Examiner in signal processor 400 and cited as corresponding to elements recited by applicants in Claim 1. Specifically, display processor 500 does not include any instruction memory (instruction cache) or any vector unit, or register files, or even a vector processing unit. Because texture memory 502 is required in display processor 500 to enable it to render images, but is not required and would not be useful in signal processor 400, there would be no motivation to move texture memory 502 into signal processor 400, or include another texture memory in the signal processor. It

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would thus not be obvious to include a texture memory like texture memory 502, in signal processor 400 of Van Hook.

Moreover, applicants have amended subparagraph (d) in Claim 1 to recite that the enhanced texture cache "is configured to store multiple partitions that are of differing lengths, to enable storage of the different types of multimedia data." Support for this amendment is provided by applicants' specification at page 12, lines 10-21, and at page 13, lines 9-23.

Texture memory 502 in Van Hook clearly does not meet this new requirement of Claim 1. Although column 52, lines 24 – 56 of Van Hook describe texture memory 502 and explain that it is used for caching an image in terms of 4-bit, 8-bit, or 16-bit textures, which are of different lengths, there is no mention or suggestion of storing multiple partitions of ***different types of multimedia data*** in texture memory 502 of Van Hook's display processor. The Examiner is cautioned about inferring that because texture memory 502 can store different length textures, one of ordinary skill in the art would find it obvious to store multiple partitions of different types of multimedia data in the texture memory. Van Hook teaches that texture memory 502 is only used to store textures for images – there is no teaching or suggestion that this texture memory is used for storing any other type of multimedia data. Further, texture memory 502 is part of display processor 500 and is not part of signal processor 400. There is no reason to assert that it would be obvious to add a texture memory 502 to signal processor 400, since the signal processor is NOT used for ***rendering*** an image or for rendering other types of multimedia data. Instead, signal processor 400 is used for other purposes, for example, carrying out matrix transforms and providing commands to display processor 500. In connection with its intended function, signal processor 400 would not benefit from inclusion of any form of texture memory, since it is not used for ***rendering*** multimedia data.

Ezer also fails to disclose an enhanced texture cache or an equivalent, that is configured to store ***multiple partitions of different lengths*** for enabling storage of different types of multimedia data. Ezer also includes a separate signal processor 202 and display processor 203. In Ezer, a texture memory 425 is used for sourcing image data used for texturing, and also "for motion compensation pertaining to MPEG." Column 8, lines 35 -36 teach that "texture memory 425 is shared between texture mapping and MPEG video processing." However, Ezer does not teach that the texture memory 425 is configured or able to store *multiple partitions of differing lengths*, to enable storage of different types of multimedia data. There is no teaching or suggestion in Ezer that the texture

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memory is even capable of storing multiple partitions of differing lengths. Thus, even if, *arguendo*, the signal processor of Van Hook were modified to include a texture memory like that of Ezer, the result would not be an equivalent of what applicants recite in Claim 1.

Since the different meanings for the same term may give rise to a misunderstanding, the Examiner should note that Ezer uses the words "partition," "partitions," and "partitioning" in a different sense than the term "multiple partitions" that is recited in applicants' claims. As explained at column 9, lines 3 of Ezer, each video time frame being processed is *partitioned* into three sequentially processed data partitions. Ezer explains that the first partition is used to perform video functions, the second partition is used to perform audio functions, and the third partition is used to perform 3-D graphics functions. Thus, Ezer refers to partitions in the sense of different sequentially processed components of a video time frame – but not in the sense of multiple segments (i.e., partitions) of differing length, for different types of data. Ezer processes the three partitions of a video time frame sequentially. In contrast, applicants recite storing multiple partitions of multimedia data in an enhanced texture cache. It should thus be evident that the partitions processed by the signal processor in Ezer are entirely different in concept than the multiple partitions of multimedia data stored in the enhanced texture cache of the programmable graphics pipeline defined in applicants' claims.

Since Van Hook discloses a signal processor 400 to provide signal processing of different types of data, but uses a display processor 500 to render only image data, and since both Van Hook and Ezer fail to teach an enhanced texture cache like that recited in applicants' claims, it should be apparent that Claim 1 defines a novel and non-obvious programmable graphics pipeline that is patentable. Since dependent claims are patentable for at least the same reasons as the independent claim on which they depend, Claims 3-16 are patentable over the art cited for at least the same reasons as noted above in regard to Claim 1.

Rejection of Claim 3-9

Claims 3-9 are rejected as unpatentable over Van Hook in view of Ezer and further in view of Gossett (U.S. Patent No. 6,104,415). The Examiner asserts that Van Hook and Ezer teach all of the limitations of Claim 3, except that the texture cache includes a line buffer and cache areas, and that the graphics pipeline further includes a texture address unit in communication with the texture cache. Applicants again disagree with this conclusion and request that the Examiner more fully clarify where

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Gossett teaches or suggests "a line buffer providing multiple read ports for accessing texture cache area." The Examiner asserts that this feature of applicants' claims is taught at column 12, lines 13-17 of Gossett, but that is not the case, as is evident from the following quote from that portion of Gossett.

> The textures originate from the SDRAM 50, and are loaded along the 256-bit bus 77 into the format unit 76, which expands or compresses the formats depending upon in what format the texture was stored. Then, a portion of that texture image is loaded into the texture cache 74. (Gossett, Column 12, line 13-17.)

Neither the above-quoted portion, nor any other portion of Gossett refers to a line buffer. Gossett does imply including a line buffer as part of the texture cache 74, but there is no indication that any equivalent of a line buffer either implicitly or explicitly provides multiple read ports for accessing multimedia data.

Applicants have also amended Claim 3 to recite a memory and an output buffer and have amended subparagraph (b) of the claim to recite "said cache area storing the multimedia data received from the memory and the output buffer." Support for this amendment is provided in applicants' specification at page 14, line 38 through page 15, line 2, and in FIGURE 3 (in this Figure, note the sources of the arrows directed to each side of enhanced texture cache 58). Gossett clearly does not teach or suggest that texture cache 74 has any capability or connection for receiving multimedia data from both a memory and an output buffer. Therefore, the Examiner's proposed combination of references neither teaches nor suggests all of the elements of dependent Claim 3, particularly as amended, and Claim 3 is also patentable for these additional reasons.

In consideration of the amendments and Remarks set forth above, it will be apparent that the claims in this application define a novel and non-obvious invention, and that the application is in condition for allowance and should be passed to issue without further delay. Should any further questions remain, the Examiner is invited to telephone applicants' attorney at the number listed below.

Respectfully submitted,

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